DECLARATION UNDER 37 C.F.R. § 1.132

Dear Commissioner:

I, Jayanta Bhadra, a resident of the city of Austin in the State of Texas , hereby state and declare as follows:

1. I am an engineer employed by the Semiconductor Products Sector of Motorola Inc. in Austin, TX.

2. I co-authored a technical paper with Magdy Abadir and Jacob A. Abraham entitled "A Quick and Inexpensive Method to Identify False Critical Paths Using ATPG Techniques: An Experiment With A PowerPC Microprocessor" that was first published on May 21, 2000 at the IEEE Custom Integrated Circuits Conference held in Orlando, Florida, U.S.

3. On February 13, 2001 I filed U.S. Patent Application Serial No. 09/781,492 entitled "Design Analysis Tool For Path Extraction And False Path Identification And Method Thereof" having claims 1-31. This patent application named myself, Magdy Abadir and Jing Zeng as inventors of the claimed subject matter.

4. All subject matter that is common between the technical paper entitled "A Quick and Inexpensive Method to Identify False Critical Paths Using ATPG Techniques: An Experiment With A PowerPC Microprocessor" and the claimed subject matter of U.S. Patent Application Serial No. 09/781,492 is solely attributable to myself and Magdy Abadir. The technical paper also listed Jacob A. Abraham as a co-author. However, Jacob A. Abraham did not contribute to any of the content of the technical paper that is common with U.S. Patent Application Serial No. 09/781,492.

5. U.S. Patent Application Serial No. 09/781,492 was filed within one year of the publication of the technical paper entitled "A Quick and Inexpensive Method to Identify False Critical Paths Using ATPG Techniques: An Experiment With A PowerPC Microprocessor".

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. Executed on the date below in Austin, Texas.

Respectfully submitted,

NOV 07, 2003

Date

Jayanta Bhadra